L10: Entry 9 of 11 File: USPT May 25, 1993

DOCUMENT-IDENTIFIER: US 5214769 A
** See image for Certificate of Correction **
TITLE: Multiprocessor control system

Detailed Description Text (9):
The MCU 11-0 comprises address registers (A-REG) 12-0, 12-1, 12-2, and 12-3, in which request information including address information for each MSU is set, and a priority order determination circuit 13-0 wherein bank busy checks and bus conflict checks or the like are executed, and which determines the access priority order to the MSU. In addition, the MCU 11-0 includes local request ports (LP0, LP1) 14-0 and 14-1 which receive requests from the PEs 17-0 and 17-1 belonging to the same MCU, and remote request ports (RP0, RP1) 15-0 and 15-1 which receive requests from the PEs 17-2 and 17-3 belonging to the other MCU 11-1.

Detailed Description Text (22):
This priority order determination circuit comprises request queues 40, request ports 41, bank conflict checkers 42, a bus conflict checker 43, a main priority order control circuit 44, and MSU address registers 12.

Detailed Description Text (23):
The four request queues 40 receive request inputs LP0, LP1, RP0, and RP1 from the processing units PE0 to PE3. The request queues 40 comprise first-in-first-out (FIFO) type register groups, and the requests set in each FIFO are supplied to the request ports 41. The outputs from each request port 41 are transmitted to the bank conflict checkers 42 and a bus conflict checker 43. The bank is a unit of division in the MSU. The bank conflict checkers 42 check the bank busy states, and the bus conflict checker 43 checks the bus conflict state. Each bank conflict checker 42 is provided with a busy flag in each memory bank, to designate a busy or not busy state.

Detailed Description Text (24):
Each bank conflict checker 42 and the bus conflict checker 43 process the requests from the local PEs in the same way as the requests from the remote PEs.

Detailed Description Text (25):
The main priority order control circuit 44 controls access requests output to the MSU, based on the check result signals received from the bank conflict checker 42 and the bus conflict checker 43. Note, the request actually picked up in the main priority order control circuit 44 and output therefrom to the MSU address registers is that from a local PE0 or PE1, and the requests from the remote PEs are picked up but not output to the MSU address registers 12. When the check results from the bank conflict checker 42 and the bus conflict checker 43 show that access to the MSU is possible, a valid bit of the corresponding address register 12 in the MSUs 10-0 to 10-3 is turned "ON" and the access request is transmitted to the MSU.

Detailed Description Text (29):
When the valid bit of the request is turned "ON" in the request port 41 corresponding to the local PE0, the bank busy and bus conflict checks are started.

Detailed Description Text (39):

If the request passes the bank busy check and the bus conflict check, the corresponding flip-flop (FF) indicating the busy state is set. The flip-flop is located in the bank conflict checker 42.

Detailed Description Text (58):
In this embodiment, all requests are transmitted to all of the main storage control units through the control bus 16, and all the main storage control units control the bank busy check and the bus conflict check in exactly the same way. Therefore, each main storage control unit can independently process the request execution for a processing unit of a main storage control unit which it controls. Further, the busy state is indicated simultaneously in all main storage control units. The accessed data is transmitted to the processing unit directly through the main storage control unit which the MCU controls, and as a result, the control is greatly simplified. The plurality of main storage control units have the same construction and each unit can be constructed by the same hardware.

CLAIMS:

3. A multiprocessor control system according to claim 1, wherein said priority order determination circuit comprises:

a plurality of bank conflict checkers for controlling use of said main storage unit and providing outputs;

a bus conflict checker for controlling common bus use; and

a main priority order control circuit controlling said main storage unit upon receipt of the outputs of said bank conflict checkers and said bus conflict checker.

6. A multiprocessor control system according to claim 5, wherein said priority order determination circuit means comprises:

request queues, operatively connected to said local request ports and said remote request ports, for receiving request inputs from said local request ports and said remote request ports;

bank conflict checkers, operatively connected to said request queues, for receiving request from said request queues for checking bank busy states;

a bus conflict checker, operatively connected to said request queues, for receiving requests from said request queues, for checking bus conflict states; and

a main priority order determination circuit connected to said bank conflict checkers, said bus conflict checker and said main storage units, for controlling access request to said main storage units in accordance with said bank conflict checkers and bus conflict checker.

11. A multiprocessor control system according to claim 10, wherein said priority order determination circuit means comprises:

request queues, operatively connected to said local request ports and said remote request ports, for receiving request inputs from said local request ports and said remote request ports;

bank conflict checkers, operatively connected to said request queues, for receiving requests from said request queues for checking bank busy states;

a bus conflict checker, operatively connected to said request queues, for receiving request from said request queues, for checking bus conflict states; and

a main priority order determination circuit connected to said bank conflict checkers, said bus conflict checker and said main storage units, for controlling access requests to said main storage units in accordance with said bank conflict checkers and bus conflict checker.

16. A multiprocessor control system according to claim 14, wherein said priority order determination circuit comprises:

a plurality of bank conflict checkers, operatively connected to said main storage units, for controlling use of a bank of one of said main storage units;

a bus conflict checker for controlling common bus use; and

a main priority order control circuit, operatively connected between said plurality of bank conflict checkers and said bus conflict checker, and said main storage units, controlling one of said main storage units upon receipt of the outputs of said bank conflict checkers and said bus conflict checker.

19. A multiprocessor control system according to claim 13, wherein said first and second priority order determination circuits each comprise:

a plurality of bank conflict checkers, operatively connected to said main storage units, for controlling use of a bank of one of said main storage units;

a bus conflict checker for controlling common bus use; and

a main priority order control circuit, operatively connected between said plurality of bank conflict checkers and said bus conflict checker, and said main storage units, controlling one of said main storage units upon receipt of outputs from said bank conflict checkers and said bus conflict checker.

23. A multiprocessor control system according to claim 21, wherein said first and second priority order determination circuits each comprise:

a plurality of bank conflict checkers, operatively connected to said main storage unit, for controlling use of a bank of each of said main storage units;

a bus conflict checker for controlling common bus use; and

a main priority order control circuit, operatively connected between said plurality of bank conflict checkers and said bus conflict checker, and said main storage units, controlling each of said main storage units upon receipt of outputs from said bank conflict checkers and said but conflict checker.

27. A multiprocessor control system according to claim 25, wherein said first and second priority order determination circuits each comprise:

a plurality of bank conflict checkers, operatively connected to said main storage units, for controlling use of a bank fo each of said main storage units;

a bus conflict checker for controlling common bus use; and

a main priority order control circuit, operatively connected between said plurality of bank conflict checkers and said bus conflict checker, and said main storage units, controlling each of said main storage units upon receipt of outputs from said bank conflict checkers and said bus conflict checker.

Refine Search

Search Results -

Terms	Documents
L4 near2 check$	11

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L10

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Thursday, May 27, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L10	l4 near2 check$	11	L10
L9	L8 same l4	5	L9
L8	bus near2 test$	2594	L8
L7	L6[ti]	11	L7
L6	bus near2 tri-state	1018	L6
L5	L4[ti]	6	L5
L4	bus near2 conflict	707	L4
L3	5594891[uref]	2	L3
L2	5420871[pn]	1	L2
L1	5373514[uref]	10	L1

END OF SEARCH HISTORY